FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: PEK-In1137 Appl. No.: Applicant: JOSEF FAZEKAS ET AL. Filing Date: August 25, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
SL	A	5,777,486	7/7/98	Hsu			
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
SL	J	06077299	3/18/94	Japan				
SL	K	2000003947	1/7/00	Japan				
SL	L	2000174085	6/23/00	Japan				
SL	M	0 448 273 A1	9/25/91	Europe				
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

SL		Schafft, H. A.: "Reliability Test Chips: NIST 33 & NIST 34 for JEDEC Inter-Laboratory Experiments and More", 97 IRW Final Report, pp. 144 and 145
SL		Sriram, T. S.: "Electromigration Test Structure Designed to Identify via Failure Modes", IEEE, 2000, pp. 155-157

EXAMINER	DATE CONSIDERED
[signature]	8/16/04